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| 09/575,561 | 05/21/2000 | Paul F. Ferguson JR. | A0312/7408/MXS | 1264 |

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| ART UNIT | PAPER NUMBER |
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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/575,561 | Applicant(s) FERGUSON ET AL. |
|---|---|---|
| | Examiner TRONG PHAN | Art Unit 2818 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Feb 20, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-52* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

***Drawings***

1. The corrected drawings received on 2/20/03 are approved.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **SC DAC 150 (lines 28 and 30, page 11).** A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: **number 152 in Figs. 5 and 13.** A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-52 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The invention as recited in claims 1-52 is not understood because of the following reasons:

a) it is not understood how the switched capacitor, the sub DACs, elements QDAC1 to QDACN and the charge sharing network in Fig. 4 are interconnected with each other since the interconnecting relationship is not described in the specification as well as is shown in any drawings of the present invention;

b) it is not understood what the SC DAC 150 as recited in lines 28 and 30, page 11 of the specification really is since it is not shown in Fig. 4 of the present invention;

c) it is not understood what the number 152 in Figs. 5 and 13 really is since it is not described in the specification; it is not understood how the P1 signal can control switch S13 (last line of page 13 and line 1 of page 14) since P1 + P2 signal is seen to be provided to switch S13 in Fig. 5; it is not understood how the P1 + P2 signal in Fig. 6 can control switch S13 in Fig. 5 since this operation is not described in the specification;

d) the switching ON/OFF operation of each of the switches in each of

Figs. 7A-C, 8A-D, 10, 11A-D, 12A-C, 14A-C, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27, 30, 33A-C and 34A-C is not understood since no P1 + P2 and P1-P3 switching control signals in Fig. 6 or P1-P4 switching control signals in Fig. 9 are seen to be respectively associated with each of the corresponding switches and the switching ON/OFF operation of each of these switches is also not described in the specification;

e) it is not understood how P1 + bit1.P2, P1 + bit2.P2, P1 + bit3.P2 and P1 + bit4.P2 control signals as shown in Fig. 31 and as described in lines 4-15, page 34 of the specification can control the switching ON/OFF operation of the corresponding switches S200-203 since the waveforms of each of P1 + bit1.P2, P1 + bit2.P2, P1 + bit3.P2 and P1 + bit4.P2 control signals are not seen in any drawings of the present invention;

f) it is not understood what all the P1-P3 signals in Fig. 32 are intended to use for applying into which corresponding switches in which respective embodiments of the present invention.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious

at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4 and 13-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633.

Fling et al., 4,591,832, discloses in Fig. 1 a system comprising:

signal preconditioner 12 for alternately providing digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver (see lines 34-36, column 2) to the common input of both DACs 16 and 18 connected in parallel (see lines 42-48, column 2); therefore, the first output analog signal 20 from the first DAC 16 is seen to be indicative of a sum of values of the input digital samples of PCM binary samples from signal preconditioner 12; and, alternately, the second output analog signal 22 from the second DAC 18 is seen to be indicative of a sum of values of the input digital samples of PCM binary samples from signal preconditioner 12 thereof;

summing circuit 24 for producing the system common output signal at terminal 25.

What is not shown in Fling et al., 4,591,832, is the multi-bit digital signal as recited in claims 1-4 and 13-51

Mehta et al., 4,205,203, discloses the teaching that digital samples of PCM binary samples are in the form of multi-bit digital signal (see the Summary of The Invention, lines 64-68, column 1 and lines 1-68, column 2).

In view of the above teaching of Mehta et al., 4,205,203, the input digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver provided to the common input of both DACs 16 and 18 in Fig. 1 of Fling et al., 4,591,832, would have been obviously in the form of multi-bit digital signal as recited in claims 1-4 and 13-51

What is not shown in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, is the signal conditioning stage comprising a switched capacitor filter as recited in claims 1-4 and 13-51

Lee et al., 6,130,633, discloses in Fig. 2A Prior Art the teaching of using switched capacitor filter 210 to be connected to the output of DAC 200.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the switched capacitor filter 210 in Fig. 2A of Lee et al., 6,130,633, for connecting to the system common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, for the purpose of performing of lowpass filtering for removal of quantization noise in the system common output analog signal at

common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203 (see lines 5-7, column 4 of Lee et al., 6,130,633).

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 5-12 and 52 are rejected under 35 U.S.C. 102(b) as being anticipated by Myers, 5,798,724.

Myers, 5,798,724, discloses in Fig. 1 Prior Art a system comprising:

finite impulse response (FIR) filter 12 for generating a sequence of N Bits digital words at an interpolation rate (see lines 14-18, column 1);

N BIT DAC 14;

reconstruct filter 16 which can be a switched capacitor filter (see lines 25-49, column 1);

as shown in Fig. 2, N BIT DAC 14 in Fig. 1 Prior Art can be implemented by the interpolating digital to analog converter 20 which includes: a first conversion stage 22 receiving an N bit data signal at an input rate (see lines 56-60, column 2)

and a second conversion stage 26 in combination with interpolation stage 30 for providing a sequence of output analog signals 32 at an interpolation output data rate which is a multiple of the input data rate (see lines 64-67, column 2) during a sampling time period/single digital and analog conversion cycle of the sampling frequency fSAMPLE of the N BIT DAC (see lines 15-24, column 3).

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Response to Arguments***

11. Applicant's arguments filed on 2/20/03 have been fully considered but they are not persuasive to place the application in condition for allowance because of the following reasons:

A) The amendments to the specification still do not mention **number 152 in Figs. 5 and 13;**

B) The amendments to the drawings still do not include the following reference sign(s) mentioned in the description: **SC DAC 150 (lines 28 and 30, page 11);**

C) The rejection under 35 USC 112, first paragraph, is still not overcome for the reasons as set forth in the above rejection under 35 USC 112, first paragraph;

D) Regarding the rejection of claims 1-4 and 13-51 under 35 USC 103(a) as unpatentable over Fling et al., 4,591,831, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633:

i) Claim 52 has been removed from the rejection under 35 USC 103(a) as unpatentable over Fling et al., 4,591,831, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633. since it depends on any of claim 5 or 12 as set forth above;

ii) Both Fling et al., 4,591,831, and Mehta et al., 4,205,203, are directed to PCM digital samples for use in system processing digital sounds

and tones. Mehta et al., 4,205,203, clearly discloses that PCM digital sample means a multi-bit binary word (see lines 56-68, column 5 of Mehta et al., 4,205,203). Therefore, the combination of Fling et al., 4,591,831, and Mehta et al., 4,205,203, is totally proper to render claims 1-4 and 13-51 obvious under 35 USC 103(a) as unpatentable over Fling et al., 4,591,831, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633;

iii) Fling et al., 4,591,831, does disclose in Fig. 2 that a first DAC 16 receiving a first input S1 having a sequence X(nt) of multi-bit digital input samples Xn-2, Xn...Xn+2 and generating a first analog output Y(nt) having a sequence of An-2, An...An+2 which is indicative of a sum values of bits in the received input multi-bit digital samples; and a second DAC 18 receiving a second input S2 having a sequence X(nt) of multi-bit digital input samples Xn-3, Xn-1, Xn+1...Xn+3 and generating a second analog output Y(nt) having a sequence of An-3, An-1, An+1...An+3 which is indicative of a sum values of bits in the received input multi-bit digital samples such as Applicant's system having "at least two analog output signals **EACH** indicative of a sum values of bits in the multi-bit digital signal" (see lines 23-25, page 4 of the original specification). More specifically, **EACH** of DACs 16 and 18 in Figs. 1-2 of Fling et al., 4,591,831 converts a sequence X(nt) of multi-bit digital input samples and generating an analog output Y(nt) having a sequence which is indicative of a sum values of bits in the received

input multi-bit digital samples. That is the fundamental characteristic of a DAC **converter- converting** all whatsoever receiving;

Accordingly, for all above reasons, the rejections of claims 1-4 and 13-51 under 35 USC 103(a) over Fling et al., 4,591,831, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633. is totally proper and is made **FINAL** as set forth above;

E) Regarding the rejection of claims 5-12 and 52 under 35 USC 102(b) as being anticipated by Myers, 5,798,724:

i) Myers, 5,798,724, does discloses the teaching of providing a sequence of output analog signals 32 at an interpolation output data rate which is a multiple of the input data rate (see lines 64-67, column 2) during a sampling time period (a single digital and analog conversion cycle) of the sampling frequency fSAMPLE of the N BIT DAC (see lines 15-24, column 3).

ii) Accordingly, the rejection of claims 5-12 and 52 under 35 USC 102(b) as being anticipated by Myers, 5,798,724, is totally proper and is made **FINAL** as set forth above.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (703) 308-4870 and email address is trong.phan@uspto.gov

March 16, 2003

phan trong

**TRONG PHAN**
**PRIMARY EXAMINER**